

Customer No.: 31561  
Application No.: 10/604,173  
Docket No.: 10873-US-PA

### AMENDMENTS

#### To the Specification:

Please amend paragraph [0009] as follows:

[0009] A display driving circuit having a plurality of driving stages and driving lines is provided. The driving stages are electrically coupled in serial, and each of the driving stages comprises a conducting path for transmitting an electric signal from the previous driving stage to the next driving stage via the current driving stage. Each of the driving lines respectively corresponds to a driving stage and electrically connects to an output terminal of the corresponding driving stage. The display driving circuit is characterized in that a redundant device is only installed in each one of redundant stages ~~a part of the driving stages~~. The redundant device is capable of supplying an extra conducting path to transmit an electric signal from the previous driving stage to the next driving stage via the current driving stage while the original conducting path in the corresponding driving stage is broken.

Please amend paragraph [0010] as follows:

[0010] In a preferred embodiment of the present invention, the redundant device is added into a redundant stage ~~driving stage~~ subsequent to a plurality of preceding driving stages that are installed separately departing from a predetermined number of the driving stages with each other. Further, the redundant device is added into a plurality of contiguous redundant ~~driving~~ driving stages

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respectively subsequent to a plurality of preceding driving stages that are installed separately departing from a predetermined number of the driving stages with each other.

Please amend paragraph [0011] as follows:

[0011] The present invention adopts a configuration of separately disposing the redundant devices in redundant stages, thus it can increase the possibility of solving the circuit malfunction problem due to the broken circuit in one aspect, and also reduce the possibility of the short circuit problem due to the redundant devices being installed in all driving stages.

Please amend paragraph [0021] as follows:

[0021] FIG. 2 schematically shows a configuration diagram of a simple system of a preferred embodiment according to the present invention. In the present embodiment, the driving circuit 20 comprises a plurality of general driving stages 202, 204, 222, and 224, a plurality of redundant driving stages 212, 214, and 232, which have redundant devices installed in them, and a plurality of driving lines 206, 208, 216, 218, 226, 228, and 234, which are electrically connected to the output terminals of the corresponding driving stages or redundant stages 202, 204, 212, 214, 222, 224, and 232. A plurality of driving stage groups 240 are electrically coupled in serial, and each of the driving stage groups 240 comprises a plurality of driving stages 202 and 204, or 222 and 224. The redundant stages 212 and 214 are alternatively disposed between the driving stage groups 240 and electrically coupled to adjacent driving stage group 240, and each

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of the redundant stages 212, 214 comprises a conducting path. Wherein, the driving stages 202 and 204 constitute a first portion of the driving circuit, and this portion of the driving circuit comprises N driving stages. The redundant driving stages 212 and 214 constitute a second portion of the driving circuit, and this portion of the driving circuit comprises M driving stages. The driving stages 222 and 224 constitute a third portion of the driving circuit, and this portion of the driving circuit comprises N driving stages, as the same as the first portion of the driving circuit. The redundant driving stage 232 constitutes a fourth portion of the driving circuit, and this portion of the driving circuit comprises M driving stages, as the same as the second portion of the driving circuit.

Please amend paragraph [0022] as follows:

[0022] Although the configuration of the present invention adds the M number of the driving redundant stages having the redundant devices subsequent to N number of the preceding general driving stages. However, it is not the only solution. It will be apparent to one of ordinary skill in the art that more driving redundant stages having the redundant devices can be disposed in the area where the poor yield rate frequently happens in the fabrication process. Contrariwise, for the area where the yield rate is better, the usage of the redundant devices should be minimized as much as possible. Therefore, the problems of the fabrication cost and the impact of the short circuit and broken circuit can be all considered.

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Please amend paragraph [0024] as follows:

[0024] FIG. 4 schematically shows a circuit diagram of a circuit suitable for use in a driving stage having a redundant device of the present invention. Wherein, the redundant device comprises six transistors 442, 444, 446, 448, 450, and 452, and these driving stages can be used as the redundant driving stages 212, 214, and 232 as shown in FIG. 2. The circuit in FIG. 4 which replaces the redundant driving stage 214 in FIG. 2, is exemplified herein for explaining the connection relationship of this circuit.

Please amend paragraph [0025] as follows:

[0025] Comparing to FIG. 3, the transistors 402, 404, 406, 408, 410, and 412 as shown in FIG. 4 are disposed on the same location of the driving stage circuit as the transistors 302, 304, 306, 308, 310, and 312 as shown in FIG. 3, respectively. Further, the transistor 442 is coupled in parallel with the transistor 402 wherein a source/drain electrode and a gate electrode are jointly electrically coupled to an inverse clock signal line XCLK; and the other source/drain electrode is electrically coupled to a source/drain electrode of the transistors 404 and 444. The transistor 444 is coupled in parallel with the transistor 404; besides a source/drain electrode is electrically coupled to the transistor 442. Its gate electrode is electrically coupled to a signal input circuit 420 that is used for inputting a signal from the redundant driving stage 212, and the other source/drain electrode is electrically coupled to a negative operating voltage VSS. A gate electrode of the transistor 446 is electrically coupled to the inverse clock signal line XCLK; a

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source/drain electrode is electrically coupled to the signal input circuit 420; and the other source/drain electrode is electrically coupled to the gate electrode of the transistors 408 and 448. The transistor 448 is coupled in parallel with the transistor 408; a gate electrode is electrically coupled to the transistor 446. Its source/drain electrode is electrically coupled to a clock signal line CLK, and the other source/drain electrode is electrically coupled to a signal output circuit 430 that is used for outputting a signal to the driving line 218. The transistor 450 is coupled in parallel with the transistor 410, and its gate electrode is electrically coupled to a source/drain electrode with which the transistor 442 and the transistor 444 are electrically coupled. Wherein a source/drain electrode is electrically coupled to the signal output circuit 430, and the other source/drain electrode is electrically coupled to the negative operating voltage VSS. The transistor 452 is coupled in parallel with the transistor 412; and its gate is electrically coupled to the inverse clock signal line XCLK, a source/drain electrode is electrically coupled to the signal output circuit 430; and the other source/drain electrode is electrically coupled to the negative operating voltage VSS.